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AMENDMENTS TO THE SPECIFICATION

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Select gates 43 are positioned between stack-gate cells 36, and a select gate 44 is positioned between the cell at one end of the group and bit line contact 46. Another select gate 45 is positioned between the cell at the other end of the group and source diffusion 51. The select gates are fabricated of a conductive material such as a doped polysilicon or polycide. They are parallel to the control gates and the floating gates, and are separated from the floating gates by dielectric films 47. As illustrated in Figure 2, the tunnel oxide 40 between the floating gates and the substrate is thinner than both the dielectric 47 between the floating gates and the select gates and the dielectric 42 between the floating gates and the control gates.

[[The]] Select gates 43, 44, 46 are separated from the substrate by gate oxide layers 53, which can be either a pure thermal oxide or a combination of thermal oxide and CVD oxide.

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As in the embodiment of Figures 2 - 4, control gates 38 cross over the floating gates 37 and isolation regions 56 in adjacent rows of cells, and select gates 43 - 45 extend in a direction perpendicular to the rows and parallel to the select gates. Bit lines 57 are perpendicular to the select and control gates, and cross over the bit line contact 46, select gates, and control gates 38 in each row of the array. The erase path once again extends from the floating gate through tunnel oxide 40 to the channel region below. As illustrated in Figure 7, the tunnel oxide 40 between the floating gates and the substrate is once again thinner than both the dielectric 47 between the floating gates and the select gates and the dielectric 42 between the floating gates and the control gates.

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NAND flash memory cell array and fabrication process in which control gates and floating gates are stacked in pairs arranged in rows between a bit line diffusion and a common source diffusion, with select gates on both sides of each of the pairs of stacked

gates. The gates in each stacked pair are self-aligned with each other and with the select gates adjacent to them. In one disclosed embodiment, the select gate at one end of each row partially overlaps the common source diffusion, and in another it lies directly above the source diffusion and is common to groups of cells on both sides of the diffusion.